Improving WLCSP Reliability Through Solder Joint Geometry Optimization

Boyd Rogers and Chris Scanlan
Deca Technologies, Inc.
7855 S. River Parkway, Suite 111
Tempe, AZ 85284 USA
Ph: 480-345-9895
Email: boyd.rogers@decatechnologies.com

Abstract
The effects of solder joint geometry on wafer-level chip-scale package reliability have been studied both through simulations and board level reliability testing. In reliability tests on a 3.9×3.9mm^2 die, an enhancement of nearly 2× in thermal cycling reliability was achieved by optimizing the solder joint and under-bump pad stack. In particular, undersizing the printed circuit board pad to produce a more spherical solder joint and reducing the polymer via size under the bump appear to be very important for improving thermal cycling results. Data collected here shows that joint geometry changes can be implemented without compromising drop performance. Methods learned were applied to the qualification of a 6.0×6.0mm^2 die, a large platform for WLCSP applications.

Key words
Board level reliability, drop testing, thermal cycling, wafer-level bumping, wafer-level chip-scale packaging

I. Introduction
Wafer-Level Chip-Scale Packaging (WLCSP) offers the smallest package form factor and has become a preferred option for the handheld consumer electronics space, where portability and increasing functionality are strong drivers. WLCSPs also continue to migrate into other applications requiring small size, high performance, and low cost. In WLCSP technology, chip I/Os are generally fanned-in across the die surface using thick polymer and redistribution line (RDL) buildup layers to produce an area array, and large solder bumps are then formed at the terminals by ball drop, solder paste printing, or plating. These additive processes allow the chip to be attached directly to a printed circuit board (PCB) with good reliability [1].

The thermal mismatch between the silicon chip and the organic PCB has limited WLCSPs to relatively small die sizes — usually less than 5×5mm^2 — so WLCSP suppliers and users are continually looking for ways to improve reliability and extend the size range of chips that can utilize this unique packaging technology. In recent years, the introduction of new polymers and solder alloys have extended the usable die sizes into the 5×5mm^2 to 6×6mm^2 range [2]–[4]. Further significant increases are likely to require new and novel WLCSP structures. materials or approaches.

Optimizing the solder joint geometry is a relatively simple but effective way to improve WLCSP reliability. Important variables to consider include the size of polymer via under the bump on the WLCSP, the size of the WLCSP under bump metallurgy (UBM) pad, and the size of the corresponding pad on the PCB. Optimizing these factors can lead to performance improvements in thermal cycling, one of the key board-level reliability tests that predict the life of the WLCSP.

In this work, the effects of solder joint geometry on WLCSP reliability have been studied both through simulations and board level reliability testing. Modeling was used to predict trends in thermal cycling performance versus changes in the geometric factors mentioned above. The predicted trends were verified by thermal cycle testing on a moderately sized WLCSP test vehicle, where an enhancement of nearly 2× in reliability was demonstrated through solder joint geometry optimization. The learnings from this study were then applied to the qualification of a 6×6mm^2 test die through thermal cycle testing and drop testing.

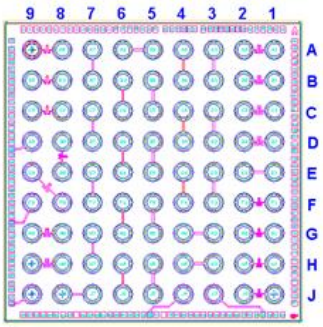


Fig. 1. 3.9×3.9mm^2 WLCSP daisy chain test vehicle

II. Test Vehicle

The test vehicle used to study the effect of solder joint geometry factors on WLCSP reliability is shown in Fig. 1. The die was 3.9×3.9mm^2, moderately sized for WLCSP applications. The WLCSP build-up layers consisted of PBO polymer and plated Cu RDL at standard industry thicknesses. The solder was SAC405, and the finished WLCSP contained 81 balls in a 9×9 array on a 0.4mm pitch. The test vehicle was a live device with RDL-level daisy chain connections that could be completed on the board side, allowing for real time monitoring during board level reliability testing.

A non-solder-mask defined solder joint, typical for WLCSP assembly, is illustrated in Fig. 2. Key aspects of the solder joint geometry are the UBM pad size on the WLCSP, the size of the polymer via under the bump on the WLCSP, and the PCB pad size. In this study, the UBM pad size was fixed at 215um and the polymer via and the PCB pad were varied to determine the effects of these changes on WLCSP performance in thermal cycling tests.

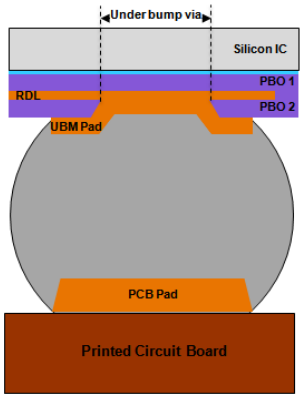


Fig. 2. Illustration of WLCSP solder joint, showing main geometric factors: UBM pad, under bump via, and PCB pad

The PCB board used in this study was an 8-layer, 1mm thick board, and the PCB pads were non-solder-mask defined. Standard JEDEC conditions were used for the temperature cycling (-40 to 125°C, 1 cycle/hr) [5]. Thermal cycling simulations were carried out assuming the above parameters, and then board level thermal cycling tests were performed to confirm the trends predicted by the simulations.

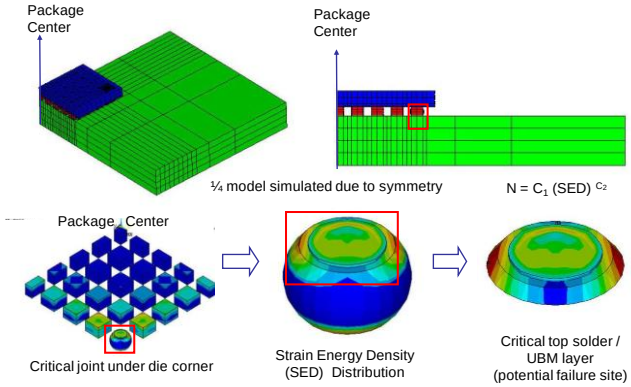


Fig. 3. ANSYS model used to simulate 0.4 mm pitch, 81 ball qualification test vehicle

III. Simulation Results

An ANSYS model, illustrated in Fig. 3, was used to simulate the thermal cycling performance of the test vehicle for various solder joint geometries. Symmetry was used to reduce the model to ¼ of the package size. For thermal cycling, the critical joint is at the corner bump, which is the furthest bump location from the neutral point, the package center. The strain energy-density-distribution (SED) for the corner bump at the bump-UBM pad interface can be used to predict the thermal cycle lifetime of the part [6], [7]. By comparing the SED for various bump geometry cases, the effects of the bump geometry on the thermal cycle lifetime was predicted.

Results of the modeling work for different bump geometries are shown in Table I. Here, the under-bump-via and the PCB pad sizes are referenced to the UBM pad, which remained fixed. The thermal cycling results are reported both as predicted cycles to first failure and as percent improvement compared to the control case. The model predicts that a smaller via under the bump is better for thermal cycling performance. The model also suggests that improvements can be obtained by choosing the proper ratio of the PCB pad to the UBM pad on the WLCSP. The PCB pad should be smaller than the UBM pad for optimized cycling performance, while a larger PCB pad results in degraded cycling performance.

Table I. Simulation predictions of thermal cycling performance for different bump geometries

Simulation Case	UBM Pad Diameter	Via Diameter	PCB Pad Diameter	Predicted Cycles to First Failure	% Improvement in TC Performance
Control	215um	0.8 x UBM pad ≈ 170um	1.0 x UBM pad = 215um	566	-
Reduced via diameter	215um	0.65 x UBM pad ≈ 140um	1.0 x UBM pad = 215um	772	36%
Reduced PCB pad diameter	215um	0.8 x UBM pad ≈ 170um	0.9 x UBM pad ≈ 190um	781	38%
Increased PCB pad diameter	215um	0.8 x UBM pad ≈ 170um	1.1 x UBM pad ≈ 135um	406	-28%

Table II. Experimental results showing thermal cycling performance for different bump geometries

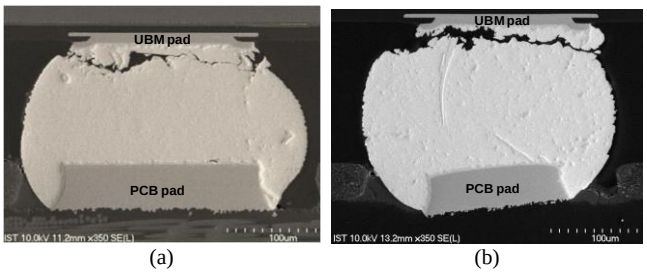
Split #	Description	Cycling Conditions (-40 to 125°C, 1 cycle/hr)	UBM Pad Diameter	Via Diameter	PCB Pad Diameter	Cycles to First Failure	% Improvement in TC Performance
1	Control	15min ramp, 15min dwell	215um	170um	215um	502	-
2	Larger via, smaller PCB pad	20min ramp, 10min dwell	215um	185um	190um	590	18%
3	Control via, smaller PCB pad	20min ramp, 10min dwell	215um	170um	190um	912	82%
4	Smaller via, smaller PCB pad	20min ramp, 10min dwell	215um	140um	190um	1003	100%

IV. Board-level Reliability Testing

Thermal cycle testing was performed using the same test vehicle and board design simulated in the modeling work. Splits were performed to test various bump geometries. In the experimental splits, the UBM pad size again remained fixed at 215um, and the under-bump-via and the PCB pad sizes were varied to produce different bump geometries.

The splits performed and the corresponding results of the board-level reliability testing are shown in Table II. Here, the trends predicted by the modeling work are confirmed: A smaller via under the bump is better for thermal cycling performance, and a smaller PCB pad compared to the UBM pad is also important for optimizing thermal cycling results. As a matter of fact, comparison of splits 1 and 3, where the via remains fixed and the PCB pad has been reduced, suggests that significant gains may be obtained in cycling performance by optimizing the ratio of the PCB pad to the UBM pad. The results suggest this ratio should be maintained at less than one for optimal cycling performance. It should be noted that these two splits were performed under slightly different cycling conditions (15min ramp and dwell for split 1 vs 20min ramp, 10 min dwell for split 3). However, modeling results suggest that the shorter dwell time will provide only ~ 7% improvement in thermal cycle performance, so most of the performance improvement is likely due to the PCB pad optimization.

SEM cross-sections of failed corner joints from splits 1 and 3 after thermal cycle testing are shown in Figs. 4(a) and 4(b), respectively. For both cases, the failure is solder fatigue, which is the desirable failure mode, and as expected, the fatigue is occurring near the bump-UBM pad interface. However, the joint from split 3 with the smaller PCB pad exhibited a significantly longer thermal cycling life than the joint from split 1. The reason for the early failure for split 1 can be understood by comparing the two photographs. In Fig. 4(a), the PCB pad is equivalent in diameter to the UBM pad. However, because the PCB pad is much thicker than the UBM pad and also is non-solder-mask defined, the wetting out of the solder around this pad during assembly causes the joint to be larger on the board side than the WLCSP side. This causes the bump to assume more of a truncated pear shape than a spherical shape and drives an earlier cycling failure near the smaller bump-UBM pad side of the joint. On the other hand, for the joint pictured in Fig. 4(b), the PCB pad is undersized compared to the UBM pad, such that the two joint sides are almost equivalent in size. This produces a more spherical-shaped bump and tends to delay the solder fatigue failure at the bump-UBM side of the joint. The smaller PCB pad also results in a little more stand-off for the WLCSP from the board, another factor in improving cycling reliability.



(a) (b)

Fig. 4. (a) SEM cross-section of failed corner bump from experimental split 1, where the PCB pad = the UBM pad.
(b) SEM cross-section of failed corner bump from experimental split 3, where the PCB pad = 0.9 x UBM pad.

The polymer via size under the bump also has a very significant effect on thermal cycling reliability, as seen by comparing splits 2, 3, and 4 in Table II. A smaller via under the bump improves cycling reliability, likely by providing more stress buffering under the bump edge. This allows the bump to 'rock' during thermal cycle stressing, with the PBO polymer under the bump absorbing more of the stress and delaying the tendency for solder fatigue failure.

In addition to thermal cycle testing, standard JEDEC drop testing was also performed on all of the experimental splits shown in Table II [8]. All splits exhibited greater than 200 drops to failure, with minimal differentiation between the splits. This suggests that the joint geometry changes discussed here can be implemented and the corresponding thermal cycling benefits obtained without compromising drop performance.

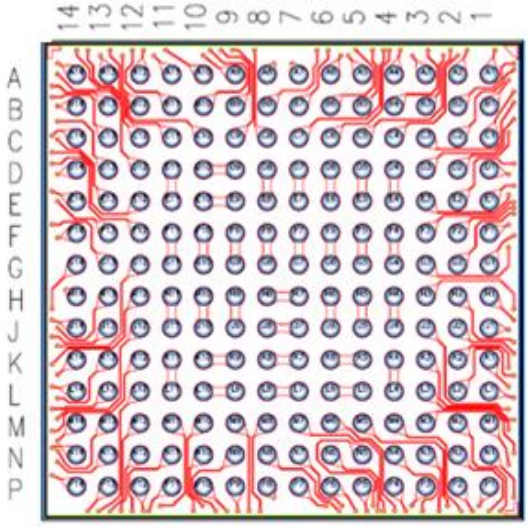


Fig. 5. 6mm × 6mm daisy chain test vehicle

V. Large Die Qualification

Solder joint optimization was next applied to the qualification of a 6×6mm^2 die. The test vehicle used is shown in Fig. 5. The WLCSP build-up layers again consisted of PBO polymer and plated Cu RDL, and the solder alloy was SAC405. The WLCSP contained 196 IOs in a 14×14 array on a 0.4mm pitch. The inner portion of the array consisted of dumbbells in the RDL layer, while the outer three rows and columns were routed through aluminum pads on the test chip.

The polymer via under the bump and the PCB pad were sized relative to the UBM pad in an attempt to maximize the reliability performance of this part. The UBM pad size was set at 240um, while the via under the bump was fixed at 180um, 75% of the UBM pad size. The board pad size was targeted at 220um, ~ 90% of the UBM pad.

The WLCSPs were again mounted on 8-layer, 1mm thick boards with non-solder-mask defined PCB pads. Fifteen parts were mounted on each board. Standard JEDEC conditions were used for the temperature cycling (method G: -40 to 125°C, 1 cycle/hr, 20min ramp, 10min dwell) [5] and drop testing (condition B: 1500Gs) [8]. Failure was defined as a 20% increase in resistance over initial values.

A Weibull plot of the thermal cycling performance for the 6×6mm^2 test die is shown in Fig. 6. The first cycling failure occurred at 560 cycles, exceeding the target of 500 cycles. The Characteristic Life of the part was 904 cycles. An SEM cross-section of a failed corner joint is shown in Fig. 7. As in the earlier study, the failure mode was solder fatigue near the bump-UBM pad interface.

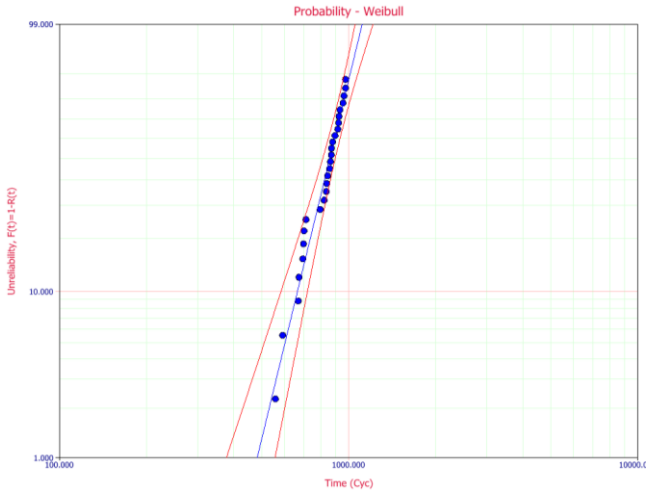


Fig. 6. Weibull plot showing thermal cycling performance of 6×6mm^2 test die. First failure is at 560 cycles and Characteristic Life of 904 cycles.

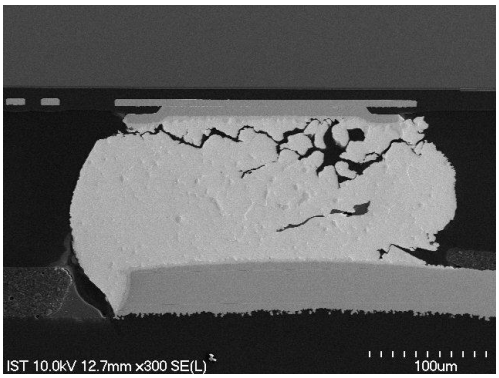


Fig. 7. SEM cross-section of a failed corner joint on 6mm × 6mm test die.

Drop testing for the 6×6mm^2 die was performed to 800 drops. Drop test results are shown in Fig. 8. The first drop failure occurred at 323 drops, well beyond the 150 drop target. While the test was not conducted to the 63.2% failure point, the Characteristic Life is predicted to be 821 drops. These results provide further evidence that the bump geometry is able to be optimized for cycling without compromising drop performance.

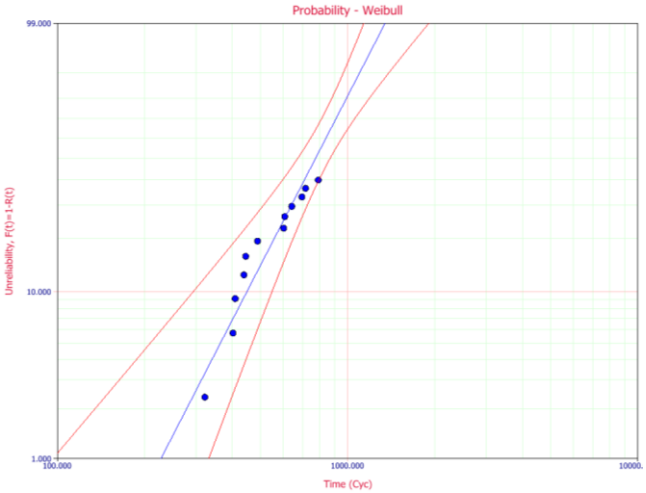


Fig. 8. Weibull plot showing drop test performance of 6×6mm^2 test die. First failure is at 323 drops, with predicted Characteristic Life of 821 drops.

VI. Conclusions

Optimizing the solder joint geometry is a simple but effective way to maximize WLCSP reliability. The results in this study suggest that a significant enhancement in thermal cycle reliability can be obtained by properly sizing the polymer via under the bump and by targeting an appropriate PCB pad to UBM pad size ratio. In particular, undersizing the PCB pad to produce a spherical joint geometry appears to be very important for optimizing thermal cycling results. In addition, this study indicates that joint optimizations to improve thermal cycling performance can be implemented without compromising drop test performance. Changes such as these can generally be implemented and performance improvements achieved without the need for introducing new materials sets and processes, often costly propositions.

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