FO-WLP Steals the Show at ECTC (/pcdesign/index.php/current-issue/234-forefront/10982-on-the-forefront-1608)

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Packed sessions highlight fan-out wafer level packaging trends.

Almost 1,500 people attended the Electronics Components and Technology Conference (ECTC) in Las Vegas to hear about the most recent trends in semiconductor packaging and assembly. ECTC opened with 18 professional development courses and an excellent special session on memory technology and prospects for packaging, featuring speakers from AMD, Intel, Rambus, SK Hynix and Xilinx.

For the second year in a row, the most heavily attended sessions focused on fan-out wafer level packages (FO-WLP). TSMC opened the first technical session with details of its integrated fan-out (InFO) wafer level system integration (WLSI) technology. The worst-kept secret in the industry is the technology is targeted for Apple's A10 processor, expected in the iPhone 7, anticipated to launch this fall. InFO will be the bottom package for the application processor, while memory will be stacked inside the top package to create a new package-on-package (PoP) format. TSMC's Through-InFO vias (TIV) are used to connect the LPDDR package on top of InFO containing the application processor, providing thinner packages than the traditional flip chip PoP (FC-PoP). TSMC released data demonstrating improved signal and power integrity, and better thermal performance than a traditional FC-PoP. TSMC reported no issues with electromigration or leakage current under high voltage bias.

Deca Technologies, which recently received a $60 million investment from ASE, provided more details of its unique maskless FO-WLP process. Deca detailed its adaptive patterning technology used to overcome the die-shift challenge that can occur when die move during the molding process. Deca uses an optical scanner to measure the position of each die after molding and generates a unique fan-out design for each package. Deca's active alignment design technique shifts and rotates the first via and fine-pitch redistribution layer (RDL) to match the die location. Adaptive routing uses a fan-out RDL design with a section removed near vias contacted to the die. Final RDL connections to the die are generated using an auto-router. Both TSMC and Deca use a chip-first process in which the chip is mounted first and the RDL created last.

ASE highlighted its many FO-WLP offerings, including the fan-out chip on substrate (FOCoS), featuring the creation of the RDL first and then chip attach. ASE also presented details of its chip-last FO-WLP for millimeter wave applications and offered a comparative study of chip-first and chip-last FO-WLP versions. Mediatek discussed a FO-WLP for a high-speed Serdes application. IME presented research on multilayer RDL for FO-WLP in mobile applications and results of a study in die shift during compression molding.

STATS ChipPAC announced cumulative shipments of 1 billion FO-WLPs in the form of the eWLB (the FO-WLP licensed from Infineon) and presented the latest on its 3D stacked eWLB, and work in conjunction with Rudolph Technologies on large-area panel processing. Ushio, in conjunction with TOK and Georgia Tech, presented work on large-area panel-level processing. Panel processing is under discussion as a cost-reduction measure for FO-WLP.

Novel FO-WLP developments were presented, including micro-transfer-printing for fan-out packaging by X-Celeprint and RTI, and the foldable FO-WLP from Fraunhofer IZM and the Technical University Berlin.

Presentations on the latest fan-in WLP developments from TSMC, Nanium, Murata Electronics, SPIL and NXP were well attended. Papers from SPIL and a joint Zymet-Cisco-Portland State University paper discussed edge bonding for WLPs to improve thermal cycling performance. Disco, Lintec and Hamamatsu discussed stealth dicing for WLP.

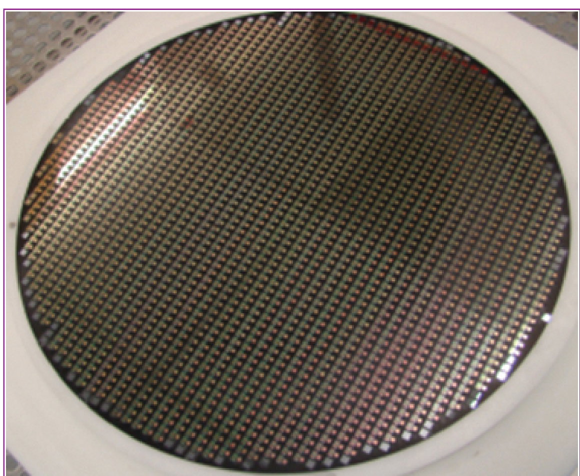

FIGURE 1. **FO-WLP is considered disruptive because it eliminates the traditional laminate substrate and underfill. (Courtesy Nanium)**

SiP saves the day. Use of an RDL to provide fine-line width and space represents the introduction of a disruptive technology because the fine-pitch RDL replaces the traditional laminate substrate. This has a major impact on the packaging and assembly infrastructure. The trend in adoption of a high-volume package without the use of a laminate substrate has resulted in a focus on substrates for system-in-package (SiP) as a growth area. While FO-WLP can also be used as SiP, the majority of today's designs use a laminate substrate. All of Friday's OSAT luncheon sponsors (JCET/STATS ChipPAC, SPIL, ASE and Amkor) highlighted their SiP capabilities.

Progress in silicon interposers and alternatives. Improvements in process, materials and assembly for 2.5D and 3DICs were highlighted with presentations from ASE, Besi, CEA-Leti, GlobalFoundries, IBM, IME, IMEC, NCAP, SK Hynix, Renesas Electronics, SPIL, Tohoku University, Xilinx and others. While progress continues, many applications are limited to the high-performance space.

AMD detailed its use of HBM stacks and logic on a silicon interposer with 65,000 TSVs. Approximately 200,000 interconnects are in the module, including Cu pillar microbumps and C4 solder bumps. The C4 bumps are used to connect the silicon interposer to the organic package substrate. Design for test (DfT) and co-design were an important part of the engineering. Bare die challenges addressed included die-to-die bonding and thin wafer handling.

eSilicon, in conjunction with Cisco, presented developments in a 3D SiP using an organic interposer for ASIC and memory integration. Unimicron updated the audience on the development of 2µm line and space embedded fine-line technology for organic interposers. Intel provided details on its embedded multi-die interconnect bridge (EMIB) package that uses a high-density piece of silicon embedded in a laminate substrate for the fine-pitch connections instead of a full silicon interposer.

The Georgia Institute of Technology (Georgia Tech), Ibiden, Xilinx and Oracle presented a joint paper on their work with embedded magnetic core inductors for high-efficiency integrated voltage regulators.

Glass: More than just for looking. Glass looks promising in applications such as RF packaging and photonics. Progress in glass substrates was highlighted by a number of companies. Atotech, Corning and Qualcomm discussed work on electroless and electrolytic copper plating of glass interposer and metal oxide adhesion for 3D RF devices. Georgia Tech discussed thermo-compression bonding on ultra-thin glass substrates and made a joint presentation with Ciena on the demonstration of glass as a superior alternative to silicon interposers for 28Gbps signal transmission. Corning discussed developments in low loss glass interposer technology. A joint paper from Koto Electric, Qualcomm and DNP provided details of a through glass metallization of direct copper-on-glass. TDK-EPCOS demonstrated an RF module design using a thin glass substrate.

Interconnect choices: Life left in wire bond. While flip chip often steals the show, K&S, NXP/Freescale and Texas Instruments focused on wire bond improvements. Infineon and Hesse discussed heavy copper wire bonding. Papers from the University of California and the University of Waterloo examined silver wire bonding.

Plenty of presentations documented progress with flip-chip bonding. TSMC presented reliability data for a 28nm device with copper pillars.

GlobalFoundries discussed reliability of copper pillars on glass and silicon interposers. IBM talked about liquid metal flip chip. IBM and Heller discussed fluxless chip joining using formic acid atmosphere for mass reflow. Amkor discussed improving copper pillar interconnection on embedded trace substrates.

IMEC discussed its small-pitch, high-aspect-ratio via-last TSV module. IME A*Star discussed the use of thermal compression bonding for 20µm Cu pillar bumps in 3D IC stacks. UTAC and IME made a joint presentation on thermal compression bonding of 30µm pitch Cu pillar microbumps. Tohoku University and GINTI detailed work on vertically stacking 20µm thick DRAM chips.

New material developments. While capillary flow remains the choice for flip chip today, several companies described new developments in mold compound as an underfill, including Panasonic's work on molded underfill for fine-pitch flip chip packages. Nonconductive film (NCF) remains a hot topic, with Dexerials introducing its NCF with non-sided filler particles. Hitachi Chemical introduced its NCF for use in thermo-compression bonding. KAIST presented on the use of a double-layer NCF for fine-pitch Cu pillar/SnAg micro-bump interconnection.

Several companies provided insight into developments specifically for power modules. Namics discussed development of a high thermal conductive adhesive film for high-performance power modules. Fraunhofer IZM and the Technical University of Berlin discussed inline monitoring of epoxy molding compound in transfer molding for smart power modules. KAIST discussed developments in anisotropic conductive film (ACF) materials. Researchers from Georgia Tech introduced work on a ceramic-metal composite filler for high thermally conductive underfill.

Singapore's Institute of Microelectronics introduced 3D graphene and 3D boron nitride networks as thermal interface materials. Dow Corning showcased its thermal interface material developments during the technology corner that featured more than 100 companies. Other materials paper highlights included:

- Brewer Science, IME, and SUSS MicroTec Lithography described the use of a new temporary bonding material for laser debonding.
- Toray Industries discussed a low-temperature positive-tone photosensitive dielectric material, pointing out the high elongation property.
- A joint paper from GE Global Research, Binghamton University and Universal Instruments explored the use of bismuth as a new Pb-free alternative for high-temperature electronics.
- Napra and Kobe University described the progress in the introduction of a nano-level SnCu die attach material for power semiconductors.
- JSR and IBM discussed the injection molded solder (IMS) option for fine-pitch flip-chip joining.

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Optoelectronics and photonics. A special session on optoelectronics featured presentations from Finisar, IBM, Luxtera, Oracle and TE Connectivity. In addition, a number of presentations focused on developments in photonics. IBM, Furukawa Electronics, Keio University and a joint presentation by Petra and AIST focused on polymer waveguides. Fraunhofer IZM and coauthors introduced a multilayer electro-optical circuit board fabricated on a large panel. Optical module developments were discussed in presentations from Oracle, Fujitsu and Oclaro Japan. A joint presentation from CEA-Leti, Nokia Bell Labs and others discussed the packaging of a high-speed coherent transmitter photonics module. IME and Nanyang Technological University discussed 3D silicon photonics packaging based on a TSV interposer for a high-density on-board optics module. Georgia Tech and Ushio discussed the design and demonstration of a micro-mirror and lens for low loss and low-cost single-mode fiber coupling in 3D glass photonic interposers. Researchers at Eindhoven University of Technology discussed development of a silicon interposer for stacking CMOS and optoelectronic dies.

MEMS, sensors and future trends explored. ECTC featured many papers on developments on MEMS and sensory technology, including a joint STMicroelectronics, EV Group, CEA-Leti presentation on 300mm wafer-level hybrid bonding for 3D stacked CMOS image sensors. With the introduction of wafer-to-wafer bonding in the latest version of Sony's image sensors, this has become a hot area. A number of presentations at ECTC and also the recent ICEP in Japan focused on direct copper bonding.

During ECTC, IMEC discussed 3D stacking using a bumpless process for sub-10µm pitch and also presented an ultra-fine pitch 3D TSV integration using a face-to-face hybrid bonding.

Emerging technology areas such as printed electronics and wearables were also discussed.

Night panels and interactive presentations. Night panel discussions included power module integration, thoughts from research institutes including University of California, Los Angeles, IMEC, IME, NCAP and CEA-Leti discussing life after Moore's Law, and a discussion on systems, devices, and packaging technologies or the IoT and the hyper-connected society. One evening session provided insights specifically for women on maximizing career potential. During the breaks, nearly 140 interactive poster sessions allowed one-on-one conversations with authors covering a wide range of topics.

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