ENHANCING WLCSP RELIABILITY THROUGH BUILD-UP STRUCTURE IMPROVEMENTS AND NEW SOLDER ALLOYS

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ABSTRACT
The effects of solder joint geometry, build-up layer thicknesses, and solder alloy composition on wafer-level chip-scale package (WLCSP) reliability have been studied through simulations and board level reliability testing. Optimizing the solder joint geometry can result in as much as a 2× improvement in thermal cycling performance. Further reliability gains can be realized by thickening up the build-up structure on the WLCSP, which can enable a significant improvement in drop performance. Combining these enhancements with an appropriate choice of solder alloy can provide a way to extend WLCSP die sizes to 6.0×6.0mm^2 and beyond.

Key words: Wafer-level chip-scale packaging, board level reliability, drop testing, thermal cycling,

INTRODUCTION
Wafer-Level Chip-Scale Packaging (WLCSP) offers the smallest package form factor and has become a preferred option for the handheld consumer electronics space, where portability and increasing functionality are strong drivers. WLCSPs also continue to migrate into other applications requiring small size, high performance, and low cost. In WLCSP technology, chip IOs are generally fanned-in across the die surface using polymer and redistribution line (RDL) buildup layers to produce an area array, and large solder bumps are then formed at the terminals by ball drop, solder paste printing, or plating. These additive processes allow the chip to be attached directly to a printed circuit board (PCB) with good reliability [1].

The thermal mismatch between the silicon chip and the organic PCB has limited WLCSPs to relatively small die sizes — usually less than 5×5mm^2 — so WLCSP suppliers and users are continually looking for ways to improve reliability and extend the size range of chips that can utilize this unique packaging technology. In recent years, the introduction of new polymers and solder alloys have extended the usable die sizes into the 5×5mm^2 to 6×6mm^2 range [2]–[4]. Further significant increases are thought to require new and novel WLCSP structures, materials or other approaches.

As has been reported previously, optimizing the solder joint geometry is a relatively simple but effective way to improve WLCSP reliability [5], [6]. Important variables to consider include the size of polymer via under the bump on the WLCSP, the size of the WLCSP under-bump-metallurgy (UBM) pad, and the size of the corresponding pad on the PCB. Optimizing these factors can lead to performance improvements in thermal cycling, one of the key board-level reliability (BLR) tests that predict the life of the WLCSP.

Further improvements in board level reliability may be obtained by optimizing the thickness of the build-up layers in the WLCSP structure [3],[7]. The polymer layers in the structure can act as buffers, absorbing stress imparted to the bumps by the chip-PCB thermal mismatch and prolonging the life of the solder joint. A common failure during drop testing is a break in the RDL layer. There is an opportunity to significantly improve reliability by increasing the thicknesses of the polymer layers and the RDL, so that the structure can better absorb the reliability stresses.

Finally, solder alloy can play a very important role in WLCSP reliability [3]. Today, a range of SAC (SnAgCu) solder alloys are available which offer significant differences in performance. Low silver alloys (~ 1% Ag) are known to perform well in drop testing, while higher silver alloys (typically 3 to 4% Ag) are generally better for thermal cycling. In recent years, alloys have been introduced with additional dopants to try to optimize both drop and cycling performance.

This work examines the relative impact of solder joint geometry, build-up layer thicknesses, and solder alloy composition on WLCSP reliability. Both modeling and board level reliability testing are used to assess the effects of various solder joint geometry factors on BLR performance, and good correlation is found between the simulation and experimental results. Then, an optimized solder joint configuration is used to study the effect of build-up layer thicknesses and solder alloy composition on the BLR performance of a large WLCSP die. Some unique, new solder alloys are included in this study which can provide significant reliability benefits if deployed in the proper context and WLCSP structure. By optimizing all three factors – joint geometry, build-up layer thicknesses, and solder alloy composition – good performance is obtained on a 6.0×6.0mm^2 die, offering the potential for qualification of even larger WLCSP platforms.

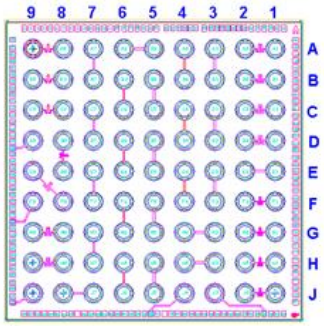


Figure 1. 3.9×3.9mm^2 WLCSP daisy chain test vehicle

SOLDER JOINT GEOMETRY OPTIMIZATION

Test Vehicle and Splits

The test vehicle used to study the effect of solder joint geometry factors on WLCSP reliability is shown in Figure 1. The die was 3.9×3.9mm^2, moderately sized for WLCSP applications. The WLCSP build-up layers consisted of PBO polymer, plated Cu RDL and a plated Cu UBM at standard industry thicknesses. The solder was SAC405 ($Sn_{95.5}Ag_{4.0}Cu_{0.5}$), and the finished WLCSP contained 81 balls in a 9×9 array on a 0.4mm pitch. The test vehicle was a live device with RDL-level daisy chain connections that could be completed on the board side, allowing for real time monitoring during board level reliability testing.

A non-solder-mask defined solder joint, typical for WLCSP assembly, is illustrated in Figure 2. Key aspects of the solder joint geometry are the UBM pad size on the WLCSP, the size of the polymer via under the bump on the WLCSP, and the PCB pad size. For the solder joint optimization study, the UBM pad size was fixed at 215um and the polymer via and the PCB pad were varied to determine the effects of these factors on WLCSP performance in thermal cycling tests.

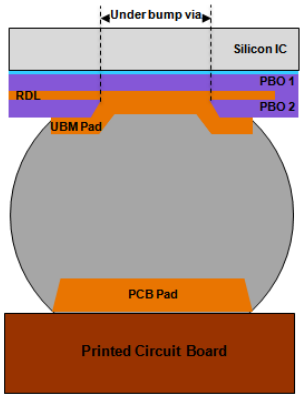


Figure 2. Illustration of WLCSP solder joint, showing main geometric factors: UBM pad, under bump via, and PCB pad

The BLR PCB used in this study was an 8-layer, 1mm thick board, and the PCB pads were non-solder-mask defined. Standard JEDEC conditions were used for the temperature cycling (-40 to 125°C, 1 cycle/hr) [8]. Thermal cycling simulations were carried out assuming the above parameters, and then board level thermal cycling tests were performed to confirm the trends predicted by the simulations.

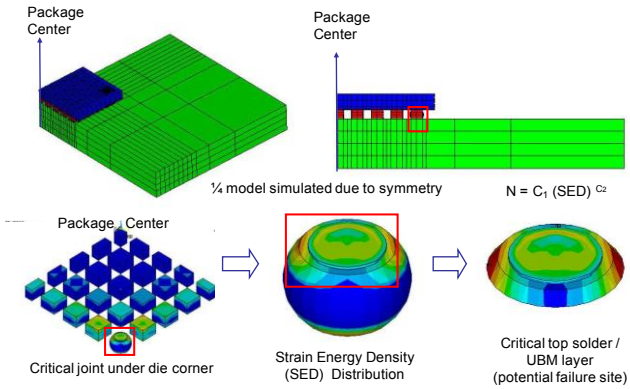


Figure 3. ANSYS model used to simulate 0.4 mm pitch, 81 ball qualification test vehicle

Simulation Results

An ANSYS model, illustrated in Figure 3, was used to simulate the thermal cycling performance of the test vehicle for various solder joint geometries. Symmetry was used to reduce the model to ¼ of the package size. For thermal cycling, the critical joint is at the corner bump, which is the furthest bump location from the neutral point, the package center. The strain energy-density-distribution (SED) for the corner bump at the bump-UBM pad interface can be used to predict the thermal cycle lifetime of the part [9], [10]. By comparing the SED for various bump geometry cases, the effects of the bump geometry on the thermal cycle lifetime was predicted.

Results of the modeling work for different bump geometries are shown in Table 1. Here, the under-bump-via and the PCB pad sizes are referenced to the UBM pad, which remained fixed. The thermal cycling results are reported both as predicted cycles to first failure and as percent improvement compared to the control case. The model predicts that a smaller via under the bump is better for thermal cycling performance. The model also suggests that choosing the proper ratio of PCB pad to UBM pad is important. The PCB pad should be smaller than the UBM pad for optimized cycling performance, while a larger PCB pad results in degraded cycling performance.

Table 1. Simulation predictions of thermal cycling performance for different bump geometries

Simulation Case	UBM Pad Diameter (um)	Via Diameter	PCB Pad Diameter	Predicted Cycles to First Failure	% Improvement in TC Performance
Control	215	0.8 x UBM pad ≈ 170um	1.0 x UBM pad = 215um	566	-
Reduced via diameter	215	0.65 x UBM pad ≈ 140um	1.0 x UBM pad = 215um	772	36%
Reduced PCB pad diameter	215	0.8 x UBM pad ≈ 170um	0.9 x UBM pad ≈ 190um	781	38%
Increased PCB pad diameter	215	0.8 x UBM pad ≈ 170um	1.1 x UBM pad ≈ 135um	406	-28%

Table 2. Experimental results showing thermal cycling performance for different bump geometries

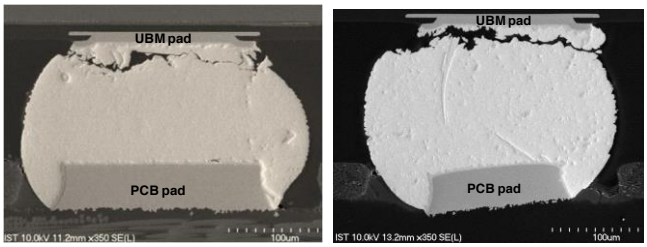
Split #	Description	Cycling Conditions (-40 to 125°C, 1 cycle/hr)	UBM Pad Diameter	Via Diameter	PCB Pad Diameter	Cycles to First Failure	% Improvement in TC Performance
1	Control	15min ramp, 15min dwell	215um	170um	215um	502	-
2	Larger via, smaller PCB pad	20min ramp, 10min dwell	215um	185um	190um	590	18%
3	Control via, smaller PCB pad	20min ramp, 10min dwell	215um	170um	190um	912	82%
4	Smaller via, smaller PCB pad	20min ramp, 10min dwell	215um	140um	190um	1003	100%

Board Level Reliability Testing

Thermal cycle testing was performed using the same test vehicle and board design simulated in the modeling work. Splits were carried out to test various bump geometries. As in the simulation tests, the UBM pad size remained fixed at 215um, while the under-bump-via and the PCB pad sizes were varied.

The splits performed and the corresponding results of the board-level reliability testing are shown in Table 2. Here, the trends predicted by the modeling work are confirmed: A smaller via under the bump is better for thermal cycling performance, and a smaller PCB pad compared to the UBM pad also improves thermal cycling results. In fact, comparison of splits 1 and 3, where the via remains fixed and the PCB pad has been reduced, suggests that significant gains may be obtained by optimizing the ratio of the PCB pad to the UBM pad. The results suggest this ratio should be maintained at less than one for optimal cycling performance. It should be noted that these two splits were performed under slightly different cycling conditions (15min ramp and dwell for split 1 vs 20min ramp, 10 min dwell for split 3). However, modeling results suggest that the shorter dwell time will provide only ~ 7% improvement in thermal cycle performance, so most of the performance improvement is likely due to the PCB pad optimization.

SEM cross-sections of failed corner joints from splits 1 and 3 after thermal cycle testing are shown in Figs. 4(a) and 4(b), respectively. For both cases, the failure is solder fatigue, the desired failure mode, and as expected, the fatigue is occurring near the bump-UBM pad interface. However, the joint from split 3 with the smaller PCB pad exhibited a significantly longer thermal cycling life than the joint from split 1. The reason for the early failure for split 1 can be understood by comparing the two photographs. In Figure 4(a), the PCB pad is equivalent in diameter to the UBM pad. However, because the PCB pad is much thicker and also is non-solder-mask defined, the wetting out of the solder around this pad causes the joint to be larger on the board side than the WLCSP side. This causes the bump to assume a truncated pear shape rather than a spherical shape and drives an earlier cycling failure near the smaller UBM pad side of the joint. On the other hand, for the joint pictured in Fig. 4(b), the PCB pad is undersized compared to the UBM pad, so that the two joints are almost equivalent in size. This produces a more spherical-shaped bump and tends to delay the solder fatigue failure at the UBM side of the joint. The smaller PCB pad also results in a little more stand-off for the WLCSP from the board, another factor in improving cycling reliability.



(a) (b)

Figure 4. (a) SEM cross-section of failed corner bump from experimental split 1, where the PCB pad = the UBM pad. (b) SEM cross-section of failed corner bump from experimental split 3, where the PCB pad = 0.9 x UBM pad.

The polymer via size under the bump also has a significant effect on thermal cycling performance, as seen by comparing splits 2, 3, and 4 in Table 2. The smaller via improves cycling reliability, likely by providing more stress buffering under the bump edge. This allows the bump to 'rock' during thermal cycle stressing, with the PBO polymer under the bump absorbing more of the stress and delaying the tendency for solder fatigue failure.

In addition to thermal cycle testing, standard JEDEC drop testing was also performed on all of the experimental splits shown in Table 2 [11]. All splits exhibited greater than 200 drops to failure, with minimal differentiation between the splits. This suggests that the joint geometry changes discussed here can be implemented and the corresponding thermal cycling benefits obtained without compromising drop performance.

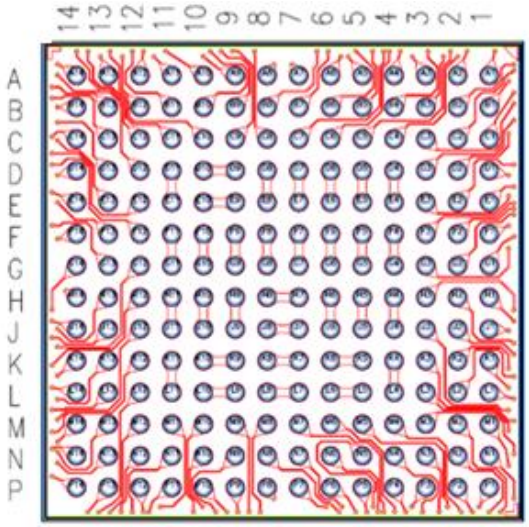


Figure 5. 6mm × 6mm daisy chain test vehicle

STRUCTURE THICKNESS AND SOLDER ALLOY OPTIMIZATION

Test Vehicle and Splits

Build-up structure thicknesses and solder alloys were next studied in an attempt to obtain further BLR performance improvements. The test vehicle used for this part of the study is shown in Figure 5. The WLCSP consisted of a 6×6mm^2 die, a large platform for WLCSP applications. The test vehicle contained 196 IOs in a 14×14 array on a 0.4mm pitch. The inner portion of the array consisted of dumbbells in the RDL layer, while the outer three rows and columns were routed through aluminum pads on the test chip.

Building on the previous solder joint optimization results, the polymer via under the bump and the PCB pad were sized relative to the UBM pad to maximize the reliability performance of this part. The UBM pad size was set at 240um, while the via under the bump was fixed at 180um, 75% of the UBM pad size. The board pad size was targeted at 215um, ~ 90% of the UBM pad.

WLCSP build-up structure thicknesses examined are illustrated in Figure 6. The standard structure consisted of PBO polymer, plated Cu RDL and a plated Cu UBM at nominal industry thicknesses. An alternative structure employing a thicker Cu RDL and PBO 2 layer was also included, to determine the potential benefits of the thicker layers on BLR performance.

Solder alloys tested are shown in Table 3. SAC405 was used as the control case. This was compared against low Ag alloys from three vendors, one containing Mn, a second containing proprietary additives, and a third containing Bi and other additives. Two new high tensile strength alloys

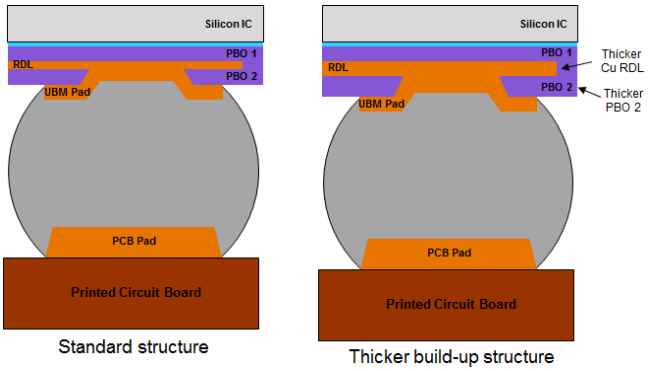


Figure 6. WLCSP build-up structure thicknesses tested

were also included, both exhibiting Vicker's Hardness values of about 2× the other alloys [12]. One of the high tensile strength alloys was doped with Bi and Ni, while the other contained undisclosed proprietary components.

Full DOE splits for this part of the study are shown in Table 4. All solder alloys were tested in the context of both build-up structures.

After fabrication of the parts shown in Table 4, solder shears were performed to compare the relative modulus of the solder alloys. Shear strength values for the different alloys are shown in Figure 7. As expected, the low silver alloys exhibited slightly lower shear strengths than SAC405, the control case, while the two high tensile strength solders exhibited significantly higher shear values.

Table 3. Solder alloys used in the 6×6mm^2 test vehicle

Solder Alloy	Supplier	Description
1	A	SAC405
2	A	Low Ag SAC alloy containing Mn
3	B	Low Ag SAC alloy containing proprietary additives
4	C	Low Ag SAC alloy containing Bi and other proprietary additives
5	C	High yield strength, high tensile strength SAC alloy containing Bi, Ni, and other proprietary additives
6	D	High yield strength, high tensile strength SAC alloy containing proprietary additives

Table 4. Full DOE splits for the alloy and build-up layer study

Split #	WLCSP Build-up Structure	Solder Alloy
1	Standard	(1) SAC405
2		(2) Low Ag SAC (Mn)
3		(3) Low Ag SAC
4		(4) Low Ag SAC (Bi)
5		(5) High tensile strength SAC (Bi, Ni)
6		(6) High tensile strength SAC
7	Thicker Cu RDL and PBO 2	(1) SAC405
8		(2) Low Ag SAC (Mn)
9		(3) Low Ag SAC
10		(4) Low Ag SAC (Bi)
11		(5) High tensile strength SAC (Bi, Ni)
12		(6) High tensile strength SAC

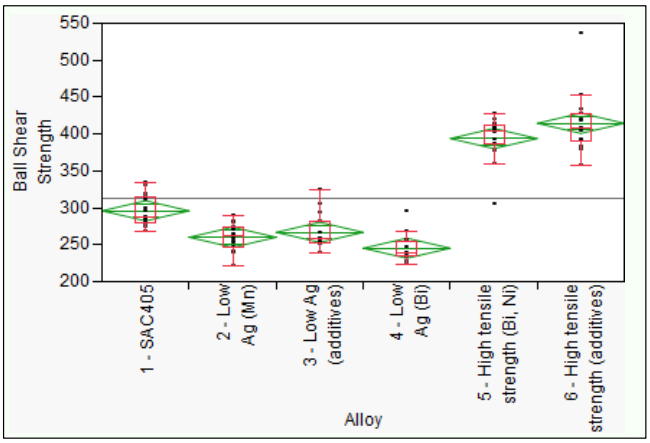


Figure 7. Solder shear performance for the different alloys

For board level reliability testing, the WLCSPs were again mounted on 8-layer, 1mm thick boards with non-solder-mask defined PCB pads. Fifteen parts were mounted on each board. Standard JEDEC conditions were used for the temperature cycling (method G: -40 to 125°C, 1 cycle/hr, 20min ramp, 10min dwell) [8] and drop testing (condition B: 1500Gs) [11]. The parts were carried to 1000 cycles or 1000 drops. Failure was defined as a 20% increase in resistance over initial values.

Thermal Cycling Results

Thermal cycling results for the various splits are shown in Table 5. Weibull plots for the standard structure and the thicker structure are shown in Figures 8 and 9, respectively.

The high tensile strength solders performed very well in thermal cycle testing. For the standard structure, both exceeded 500 cycles to first failure, and, in fact, alloy #5 doped with Bi and Ni exhibited no failures out to 1000 cycles. With the thicker build-up structure, only one failure was recorded for the two high tensile alloys combined, with a first failure of 987 cycles for the version doped with Bi and Ni. The benefit of the thicker build-up structure on high tensile strength alloy #6 was very significant, moving the first failure from 531 cycles to over 1000 cycles.

SAC405 solder (alloy #1) also performed relatively well in thermal cycling tests. With the standard structure, this alloy exhibited a first failure at just under 500 cycles (485 cycles) and a characteristic life of 938 cycles. With the thicker build-up structure, there was a measurable improvement in first failure (614 cycles) but a similar characteristic life (944 cycles).

All of the low Ag alloys tested (alloys #2 – #4) underperformed in thermal cycle testing relative to the other alloys in this study, and there was no significant improvement in moving from the standard structure to the thicker structure.

Table 5. Thermal cycling results for the various solder alloys with the standard and thick build-up structures

Split #	WLCSP Build-up Structure	Solder Alloy	First Failure (Cycle)	Cumulative Failures at 1000 Cycles (%)	Characteristic Life (Cycles)
1	Standard	(1) SAC405	485	82%	938
2		(2) Low Ag SAC (Mn)	308	100%	578
3		(3) Low Ag SAC	383	100%	576
4		(4) Low Ag SAC (Bi)	317	100%	421
5		(5) High tensile strength SAC (Bi, Ni)	none	0%	-
6		(6) High tensile strength SAC	531	37%	1142
7	Thicker Cu RDL and PBO 2	(1) SAC405	614	73%	944
8		(2) Low Ag SAC (Mn)	218	100%	516
9		(3) Low Ag SAC	330	100%	525
10		(4) Low Ag SAC (Bi)	325	100%	473
11		(5) High tensile strength SAC (Bi, Ni)	987	3%	-
12		(6) High tensile strength SAC	none	0%	-

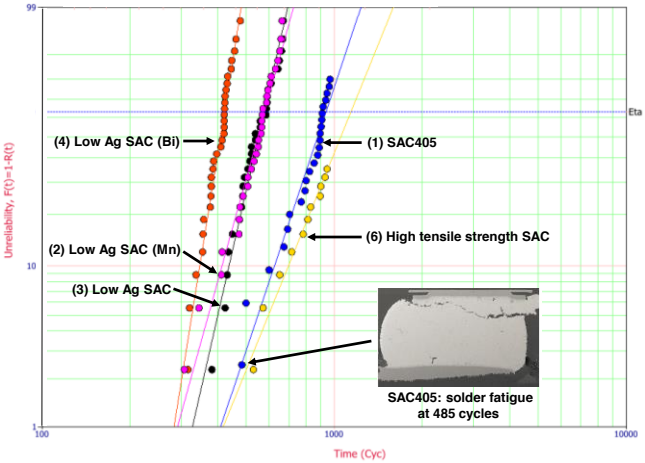


Figure 8. Weibull plots showing cycling performance for the various solder alloys using the standard build-up structure. High tensile strength alloy #5 doped with Bi and Ni is not shown because no failures were recorded.

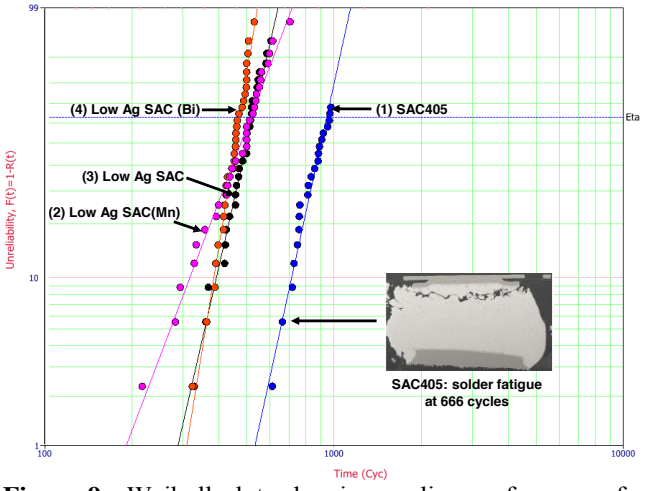


Figure 9. Weibull plots showing cycling performance for the various solder alloys using the thicker build-up thicker build-up structure. High tensile strength alloys are not shown because no failures were recorded

All in all, the improvement in cycling performance with the thicker build-up structure was insignificant for the low Ag alloys, moderate for SAC405, and moderate to very significant for the high tensile strength alloys.

The failure mode for SAC405 solder has been determined and is shown in the inserts on the two Weibull plots in Figures 8 and 9. This alloy exhibited solder fatigue failure at the corner bumps, a typical failure mode observed in temperature cycling.

Drop Test Results

Drop tests results for the various splits are shown in Table 6. Weibull plots for the standard structure and the thicker structure are shown in Figures 10 and 11, respectively.

For the standard structure, SAC405 performed very well in drop testing, with a first failure at 277 drops and a characteristic life of 902 drops. Two of the low Ag solders also performed well, with first failures of greater than 100 drops and with high characteristic lives. The third low Ag alloy (alloy #3) exhibited a relatively early failure at 56 drops and a lower characteristic life. Both high tensile strength SAC alloys suffered from relatively early drop failures. This was especially true for the alloy #5 with Bi and Ni doping. This alloy also exhibited a relatively low characteristic life. All of the Weibull plots exhibited non-linear behavior, indicating the possibility of multiple failure modes.

For the thicker structure, all alloys performed very well, exhibiting a 2× or better performance improvement when compared to the standard structure. All characteristic lives were greater than 1000 cycles, and the Weibull plots were more linear, suggesting possibly a single failure mode.

The drop failure mode for the SAC405 solder is again shown in the inserts on the two Weibull plots in Figures 10 and 11. The drop test resulted in a break in the RDL under the corner bump, which is typical in WLCSP drop testing.

DISCUSSION

The results here demonstrate that structural changes can improve WLCSP reliability and extend the working space to larger die sizes. Reducing the size of the polymer via under the bump can improve cycling performance, by providing more stress buffering under the bump edge. Undersizing the board pad relative to the UBM pad results in a more optimized spherical bump geometry. This tends to delay the solder fatigue failure at the bump-UBM side of the joint, also improving cycling performance. Finally, thickening up the RDL and polymer 2 layers can produce significant gains

Table 6. Drop test results for the various solder alloys with the standard and thick build-up structures

Split #	WLCSP Build-up Structure	Solder Alloy	First Failure (Drop)	Cumulative Failures after 1000 Drops (%)	Characteristic Life (Drops)
1	Standard	(1) SAC405	277	40%	902
2		(2) Low Ag SAC (Mn)	114	30%	2713
3		(3) Low Ag SAC	56	53%	1013
4		(4) Low Ag SAC (Bi)	155	37%	1651
5		(5) High tensile strength SAC (Bi, Ni)	20	67%	462
6		(6) High tensile strength SAC	79	40%	1133
7	Thicker Cu RDL and PBO 2	(1) SAC405	550	17%	1277
8		(2) Low Ag SAC (Mn)	215	37%	1277
9		(3) Low Ag SAC	172	37%	1583
10		(4) Low Ag SAC (Bi)	501	23%	1135
11		(5) High tensile strength SAC (Bi, Ni)	316	38%	1170
12		(6) High tensile strength SAC	197	33%	1533

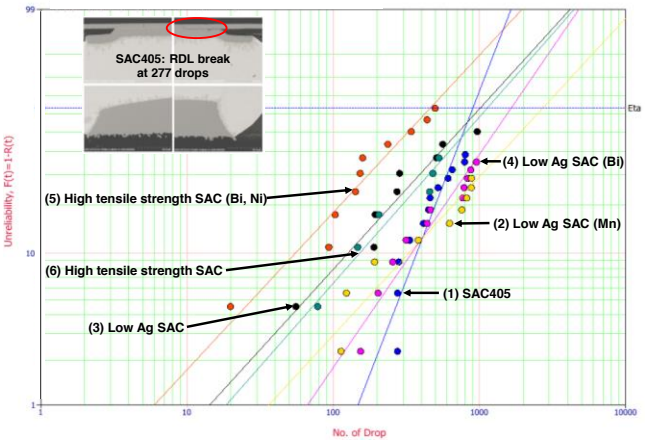


Figure 10. Weibull plots showing drop test performance for the various solder alloys using the standard build-up structure.

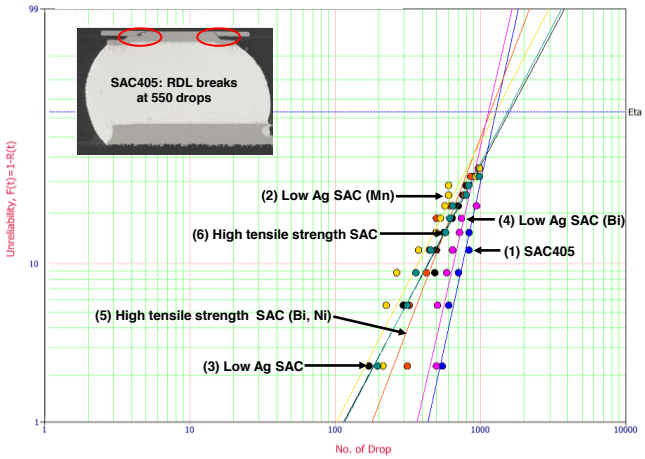


Figure 11. Weibull plots showing drop test performance for the various solder alloys using the thicker build-up structure.

in drop test performance. Drop performance is likely improved with the thicker structure because the failure mode at drop testing is typically a break in the RDL. Thickening the RDL appears to be an effective means of delaying this type of failure and extending the usable life of the part.

Selection of an appropriate solder alloy can also result in significant reliability gains. SAC405 performed well in this study in both drop and temperature cycling and continues to be a mainstay for enabling reliable parts. In particular, on the 6×6mm^2 test vehicle with the thicker structure, this alloy lasted 614 cycles and 550 drops before first failure, which are passing values according to most standards. As expected, the low Ag alloys performed well in drop testing, but these alloys tended to underperform in cycling. In all cases, these alloys were unable to reach 400 cycles to first failure and exhibited characteristic lives of less than 600 cycles on the 6×6mm^2 part.

The high tensile strength alloys appear particularly promising. These alloys exhibit very strong performance in thermal cycling, likely because they are able to delay solder fatigue, the typical cycling failure. As expected, these alloys tend to underperform in drop testing. However, when combined with the thicker build-up structure, these alloys posted very solid drop performance numbers, with first failures of greater than 195 drops and characteristic lives of more than 1000 drops. A strategy of combining an optimized joint geometry and a thicker buildup structure with a high tensile strength alloy may offer a path for extending WLCSP die sizes well beyond 6×6mm^2.

CONCLUSIONS

Optimizing the WLCSP structure is an effective way to improve WLCSP reliability. A significant enhancement in thermal cycling reliability can be obtained by reducing the polymer via under the bump and by undersizing the PCB pad relative to the UBM pad, to produce a spherical joint geometry. Also, thickening up the build-up structure on the WLCSP can result in a significant improvement in drop performance. These structural improvements can be combined with a high tensile strength solder alloy to produce a part optimized for cycling and drop, providing the potential to extend usable die sizes to 6×6mm^2 and beyond.

REFERENCES

[1] P. Garrou, “Wafer level chip scale packaging (WL-CSP): An overview,” IEEE Trans. of Adv. Packaging, 2000, Vol. 23(2), pp. 198-205.

[2] R. Chilukuri, “Technology solutions for a dynamic and diverse WLCSP market”, IWLPC Proc., San Jose, CA (2010).

[3] R. Anderson, R. Chilukuri, T. Y. Tee, C. P. Koo, H. S. NG, B. Rogers, and A. Syed, “ Advances in WLCSP technologies for growing market needs”, IWLPC Proc., San Jose, CA (2009).

[4] R. Anderson, T. Y. Tee, R. Moody, L. B. Tan, H. S. NG, J. H. Low, and B. Rogers, “Integrated testing & modeling analysis of CSPnl™ for enhanced board level reliability,” IWLPC Proc., San Jose, CA, 184-190, (2008).

[5] B. Rogers and C. Scanlan, “Solder Joint Geometry Optimization Increase WLCSP Reliability,” Chip Scale Review, Vol 17(3), pp. 41-43.

[6] B. Rogers and C. Scanlan, “Improving WLCSP Reliability through Solder Joint Geometry Optimization,” Advancing Microelectronics, Vol 41(1), pp. 14-17.

[7] R. Anderson, Robert Moody, B. Rogers, and D. Mis, “Board Level Reliability Results for Amkor’s 12x12 I/O CSPnl™”, IMAPS Proc., Scottsdale, AZ (2008).

[8] JEDEC Standard JESD22-A104C, Temperature Cycling, 2005.

[9] R. Darveaux, K. Banerji, A. Mawer, and G. Dody, “Reliability of Plastic Ball Grid Array Assembly,” Ball Grid Array Technology, J. Lau Editor, McGraw-Hill, New York, 1995, pp. 379-442.

[10] R. Darveaux, “Effect of simulation methodology on solder joint crack growth correlation,” 50th ECTC Conf. Proc., 2000, pp. 1048-1058.

[11] JEDEC Standard JESD22-B111, Board Level Drop Test Method of Components for Handheld Electronic Products, 2003.

[12] R.L. Smith and G.E. Sandland, "An Accurate Method of Determining the Hardness of Metals, with Particular Reference to Those of a High Degree of Hardness," Proceedings of the Institution of Mechanical Engineers, Vol. I, 1922, p 623–641.